IN THE ABSTRACT:

Please enter the replacement Abstract, below:

ABSTRACT OF THE DISCLOSURE

A first transparent latch receives a first synchronised signal changing its logic state synchronously with respect to a clock signal. A second transparent latch receives a second synchronised signal output by the first latch. When the clock signal has a first logic state the first latch has a non-responsive state and the second latch has a responsive state, and when the clock signal has a second logic state the first latch has the responsive state and the second latch has the non-responsive state. The change in logic state of a third synchronised signal output by the second latch is guaranteed to occur in a particular half-cycle of the clock signal, irrespective of process/voltage/temperature (PVT) variations of the circuitry. Clock recovery circuitry may have rising-edge and falling-edge latches; circulating control pattern verification circuitry; data synchronising circuitry for converting parallel data clocked by a first clock signal into serial data clocked by a second clock signal asynchronous with the first clock signal; and data recovery circuitry for producing an offset clock signal which suits a data eye shape of a received serial data stream.